A 4-8 GHz Quasi-MMIC IF Amplifier for a 690 GHz SIS Receiver

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Abstract

We are developing a 4 to 8 GHz cryogenic low-noise amplifier (LNA) using Quasi-Monolithic Microwave Integrated Circuit (QMMIC) technology. This amplifier has been demonstrated as an IF amplifier of a 690 GHz quasi-optical SIS receiver for the Caltech Submillimeter Observatory (CSO), and later will be used on SOFIA. The QMMIC consists of a thin-film passive circuit on a GaAs substrate with three 160 μm gate InP HEMTs bump-bonded to it. The measured amplifier gain is over 32 dB and noise is approximately 8 Kelvin from 4 to 8 GHz at a physical temperature of 4 Kelvin. The 690 GHz SIS receiver uses a NbTiN ground plane to achieve a measured uncorrected double-sideband noise temperature of 180 Kelvin. An isolator for the 4 to 8 GHz band was used between the mixer and IF amplifier. A room-temperature IF system has been developed with gain flat to within 1 dB in the 4 to 8 GHz band. The receiver was used at the CSO with a 4 GHz analog correlation spectrometer to detect the J=6→5 emission line of carbon monoxide from the galaxy M82.

I. Introduction

The IF systems currently in use at ground-based submillimeter observatories typically have bandwidths of 1 GHz. For the higher frequency bands, especially those available to SOFIA and FIRST, a 1 GHz bandwidth will be inadequate for observations of spectral lines from external galaxies. For example, the J=6→5 emission line of carbon monoxide from the galaxy Arp 220 has a linewidth of over 1.8 GHz. For this reason, the standard IF bandwidth for our Caltech SOFIA instrument and FIRST HIFI will be 4 GHz.

The initial reason for considering a MMIC approach to the amplifier design was to gain better control over parasitics compared to a discrete-component amplifier. However, fabrication of MMIC devices is expensive due to the presence of transistors. Choosing a quasi-MMIC approach not only greatly reduces the fabrication costs, it also permits the selection of transistors from known good wafers. Since many amplifiers will be needed for our SOFIA instrument, the CSO, etc., the relative ease of assembly associated with the QMMIC devices was also attractive. Bump-bonding the transistors creates a robust circuit free from wire bond parasitics. Other advantages of the QMMIC approach include small size and relatively easy adaptability to different packaging constraints. For example, the QMMIC amplifier could more easily be integrated into the mixer block than a discrete-component amplifier.

II. Receiver Configuration

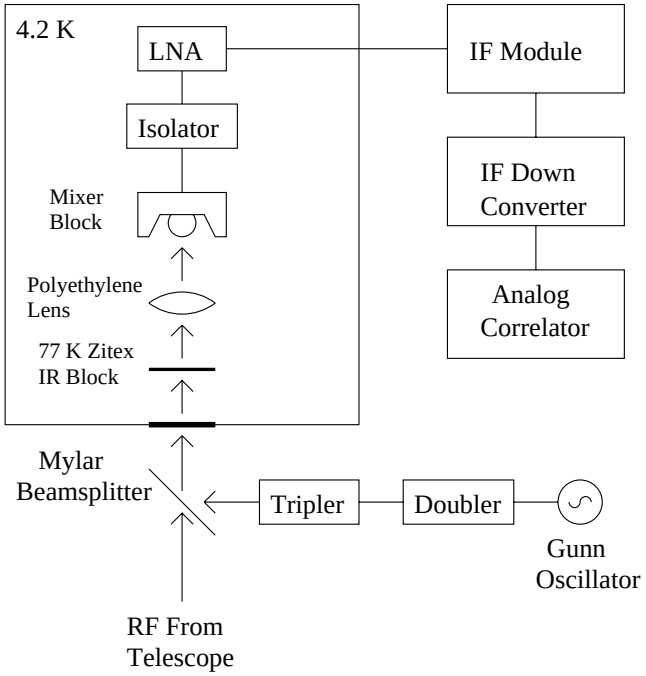

Fig. 1. Configuration of the receiver.

A block diagram of the receiver is shown in Figure 1. The local oscillator (LO) is generated by a tunable Gunn oscillator [1] and multiplied by $x2$ and $x3$ varactor multipliers [2]. The LO is combined with the RF signal through a 13 μm mylar beamsplitter, and then enters a liquid helium cryostat through a teflon–coated quartz pressure window. A 77 Kelvin Zitex filter blocks infrared radiation. The LO and signal then pass through a polyethylene lens and into a silicon hyperhemisphere antireflection coated with alumina–doped epoxy. The hyperhemispherical lens focuses the signal onto a twin–slot antenna, which is used for its nearly–circular beam profile. Since 690 GHz photons are close to the gap energy of niobium, a NbTiN ground plane (Tc=15.75 Kelvin) is used for the slot antenna to reduce losses associated with the breaking of Cooper pairs. Niobium microstrip lines over the NbTiN ground plane match the signal from the slots into a pair of Nb–AlO–Nb SIS junctions.

The IF signal is coupled out of the mixer chip through wire bonds to a duroid microstrip circuit that matches the impedance to 50 Ω. The signal then passes through a 4 to 8 GHz isolator, and into the low–noise amplifier. The signal then leaves the 4 Kelvin work surface, exits the cryostat, is amplified by a 4 to 8 GHz room–temperature stage, down–converted to 0.5 to 4.5 GHz, and analyzed by a 4 GHz analog correlation spectrometer.

III. QMMIC LNA

The amplifier was designed to operate at 4 Kelvin, with over 30 dB gain in the 4 to 8 GHz band and noise temperatures in that band below about 5 Kelvin. InP HEMTs were obtained from the Microwave and Lidar Technology Section at the Jet Propulsion Laboratory, and their scattering parameters were measured on a microwave probe station. Marian Pospieszalski's FET model [3] was then fit to these data to determine model parameters. The noise prediction from the model, given a best-guess value of the noisy drain-resistor temperature, was used without any direct measurement of the transistor noise correlation matrix. The model was used in the program SuperMix [4] [5] to simulate and evaluate different tuning circuits for the amplifier. The SuperMix software includes an optimizer, which was used to optimize the design for flat gain above 30 dB, low noise, input reflections below about -10 dB, output reflections below -20 dB, and unconditional stability at all frequencies, all while keeping total power consumption low. The DC gate and drain bias for each transistor were kept separate to reduce power consumption on the cryogenic stage and allow performance to be fine-tuned. Two designs were selected for fabrication, one optimized for best performance (Figure 2), and one optimized for greater stability.

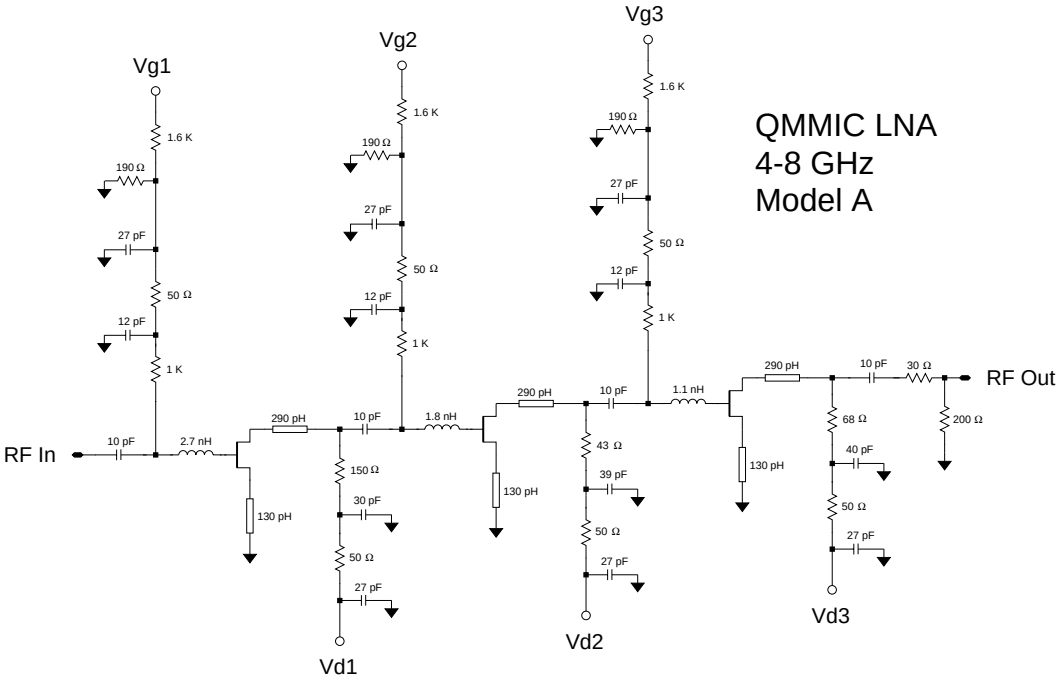

Fig. 2. Amplifier Schematic.

After the ideal circuit designs were completed, physical resistors, capacitors, and inductors were laid out. The substrate includes air bridges and a resistive layer, Table I, but for simplicity does not include via holes. Each component, including five spiral inductors, was simulated with Agilent's EM simulator, *Momentum*. Results of the EM simulations were saved as scattering parameter files which were then imported

Layer	*Thickness*
Bump Gold	8 μm
Air Bridge Gold	1 μm
Air	2 μm
SiN	296.5 pF/mm^2
Gold	1 μm
NiCr Resistor	50 Ω/square
GaAs	250 μm

TABLE I
LAYERS IN THE QMMIC SUBSTRATE.

back into SuperMix for the final simulation. The results of these simulations are plotted in Figure 3. The final mask layout is show in Figure 4.

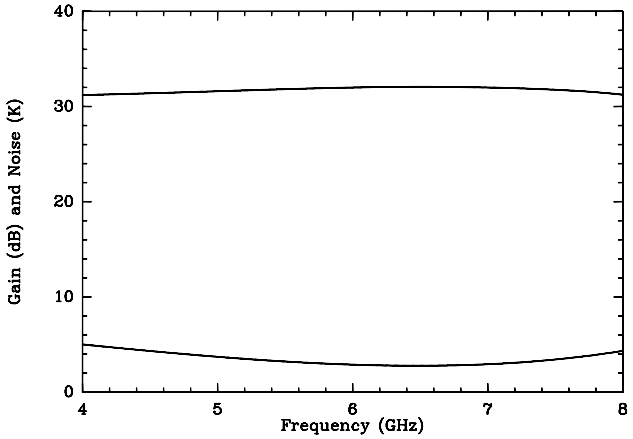

Fig. 3. Predicted gain and noise performance of the QMMIC amplifier.

The input and output of the QMMIC chip are coplanar waveguide (CPW), both to avoid via holes and to allow the devices to be tested on a probe station. A circuit was designed to convert from the QMMIC CPW to microstrip, which in turn can be soldered to SMA connector pins. The thickness and dielectric constant of these transition circuit boards were chosen to roughly match those of the QMMIC chip. Ground plane spacings for 50 Ω CPW were calculated for center conductor widths ranging from the QMMIC CPW value to that of 50 Ω microstrip. These values were used to lay out the transition circuit board. Via holes were used to connect the top and bottom ground planes. The EM simulator Momentum predicted reflections below -34 dB in the 4 to 8 GHz band for the transitions.

The amplifier housing was designed to be compact (Figure 5). The microwave and bias circuits were split into two separate cavities on opposite sides of the housing. This way, the microwave side could be kept small to eliminate in-band cavity resonances.

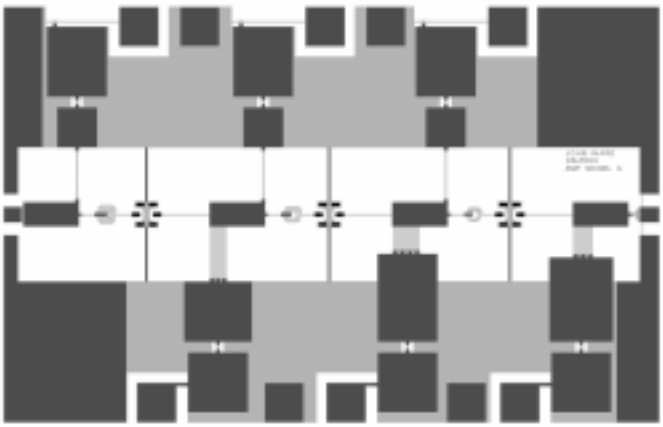

Fig. 4. Mask layout of the QMMIC substrate. Actual size is approximately 2.5x3.8 mm. The InP HEMTs are bonded to the three pads spaced horizontally across the center of the chip. The input is coplanar waveguide on the left, and the output is on the right. There are three bond pads at the top for gate bias, and three across the bottom for drain bias.

DC bias for the transistors was brought up to the microwave cavity from the DC cavity using small feed-thru pins. The DC cavity contains filtering capacitors and overvoltage protection diodes.

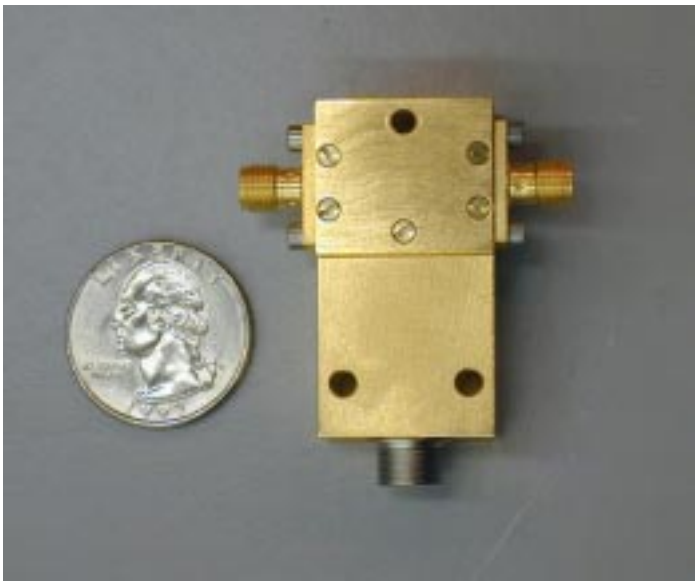

Fig. 5. The assembled amplifier. The lid between the SMA connectors covers the microwave cavity.

IV. SIS Mixer

The SIS mixer chip was originally designed and fabricated for use with a 1 to 2 GHz IF. The chip was tested with a 1 to 2 GHz IF, and then simulated using the SuperMix library. An IF matching circuit was then designed to allow the chip to be used with a 50 Ω, 4 to 8 GHz low-noise amplifier.

A. SIS Chip

A photograph of the twin slot antenna is shown in Figure 6. This type of mixer, with twin slot antenna, dual SIS junctions, and anti-reflection coated silicon hyperhemispherical lens, has already been discussed in the literature, and so won't be described in detail here. [6] [7] [8] [9]

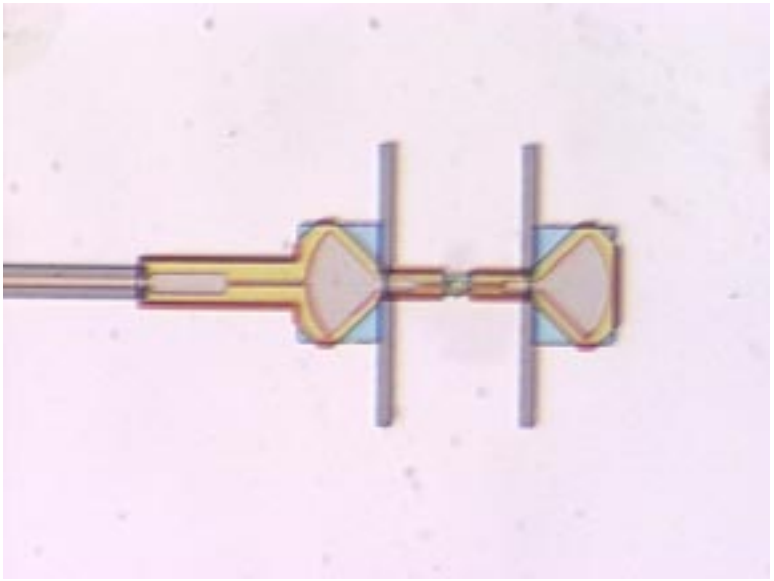

Fig. 6. The SIS chip. The RF and LO signals couple in through a silicon hyperhemisphere underneath the chip. The vertical lines are the slots. The SIS junctions are the black dots near the center of the "H." The IF signal exits through the transmission line on the left.

The mixer was first tested with a 1 to 2 GHz IF system. The unilluminated and pumped current-voltage (IV) curves were measured for a variety of LO frequencies, and the receiver response was measured with a Fourrier transform spectrometer (FTS.) The IV and FTS data were used to verify the SuperMix simulations, and to constrain the primary unknown parameter, i.e. the surface impedance of the NbTiN film.

B. IF Matching Circuit

The IF output impedance of the mixer chip was calculated with the verified SuperMix model. The IF output impedance can be well modeled as a parallel RC circuit, as shown in Figure 7. The capacitance is the combination of the chip capacitance and the quantum susceptance, while the resistance is related to the slope of the pumped IV curve at the bias point. As expected, for a fixed bias voltage and LO power, the IF impedance varies with LO frequency, Figure 8. In particular, the capacitance of the RC model stays constant, while the resistance varies. Similarly, holding the LO frequency constant while varying the LO power also causes the RC model resistance value to vary while the capacitance stays constant. It was found that varying the LO power as a function of LO frequency in a well-defined way will keep the model resistance constant, and thus hold the IF impedance constant with respect to LO fre-

quency. A receiver-tuning lookup table was created to give the target DC pumped SIS current as a function of LO frequency to keep the IF output impedance at a standard value.

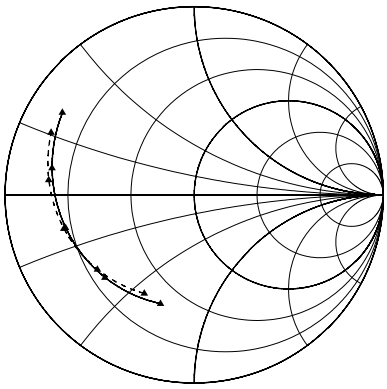

Fig. 7. IF impedance of the full SIS chip simulation compared to the simple parallel RC model. The impedance Smith chart is referred to 50 Ω. The mixer impedance (solid line) is for any LO frequency, as long as the LO power is adjusted appropriately. The parallel RC model (dashed line) is for 109 Ω and 832 fF. Note that wire bond inductance and DC blocking capacitors are included in the impedance calculations.

Several considerations had to be kept in mind while designing the IF matching circuit. First of all, the RF return loss is strongly affected by the IF impedance seen by the mixer. For some range of IF impedances, typically for a conjugate-matched IF, there can be reflection gain at the RF port. [10] Secondly, for the parallel RC impedance presented by our mixer chip, the Bode-Fano limit for the return loss matched to 50 Ω is about -6 dB for a 4 GHz bandwidth. [11] [12] [13] Finally, the primary goal of low system temperature had to be achieved while keeping the passband reasonably flat.

A 2-element microstrip circuit was designed to achieve the Bode-Fano limit for matching the mixer IF impedance to a 50 Ω line. The receiver was then simulated to see how the entire system would perform using this circuit, computing reflections at the RF ports, total receiver noise temperature including the isolator and IF amplifier, conversion loss, etc. The microstrip matching circuit had to be detuned slightly to improve the RF match and eliminate the possibility of RF reflection gain. Figure 9 shows a schematic of the matching circuit, and Figure 10 shows a photo of the assembled mixer.

V. Measurements and Results

A prototype LNA was constructed and tested at 4 Kelvin. The gain was found to be above about 32 dB, and the noise ranged from 6 to 12 Kelvin, Figure 11. The power consumption was 8 mW. The LNA was also tested at 4 Kelvin with an isolator at the input. The gain shape within band was essentially unchanged, while the noise

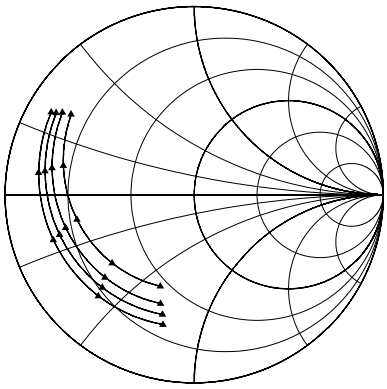

Fig. 8. IF impedance from 4 to 8 GHz of the SIS chip for various LO frequencies. The impedance Smith chart is normalized to 50 Ω. The LO frequencies are, from left to right, 640, 660, 680, and 700 GHz. The bias voltage and LO power are constant. Note that wire bond inductance and DC blocking capacitors are included in the impedance calculations.

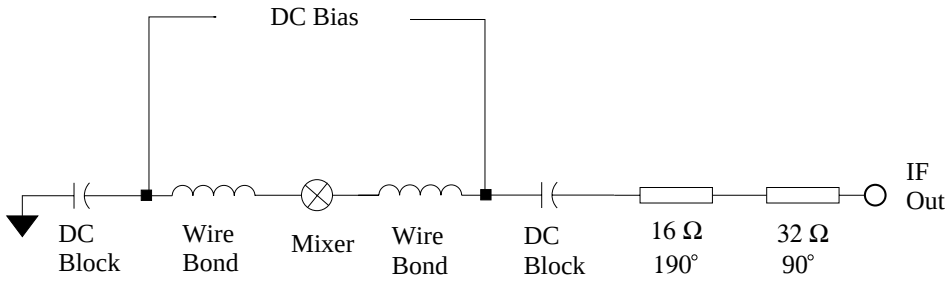

Fig. 9. Schematic diagram of the IF matching circuit, including wire bonds, DC blocking capacitors, etc.

of the amplifier increased by about 35% due to loss from the isolator and cables.

The receiver was assembled and run with the tested amplifier and isolator. Figure 12 shows the cold surface of the cryostat. The double sideband noise temperature was generally below 200 Kelvin, Figure 13. Figure 14 shows the pumped and unpumped IV curves with receiver IF output power for hot and cold RF loads.

The receiver was taken to the Caltech Submillimeter Observatory and used with a 4 GHz analog correlator provided by Andy Harris of the University of Maryland. [14] A photograph of the receiver mounted at the Cassegrain focus of the telescope is shown in Figure 15. The receiver was used to observe the J=6→5 emission line of carbon monoxide from the galaxy M82, Figure 16.

Acknowledgements

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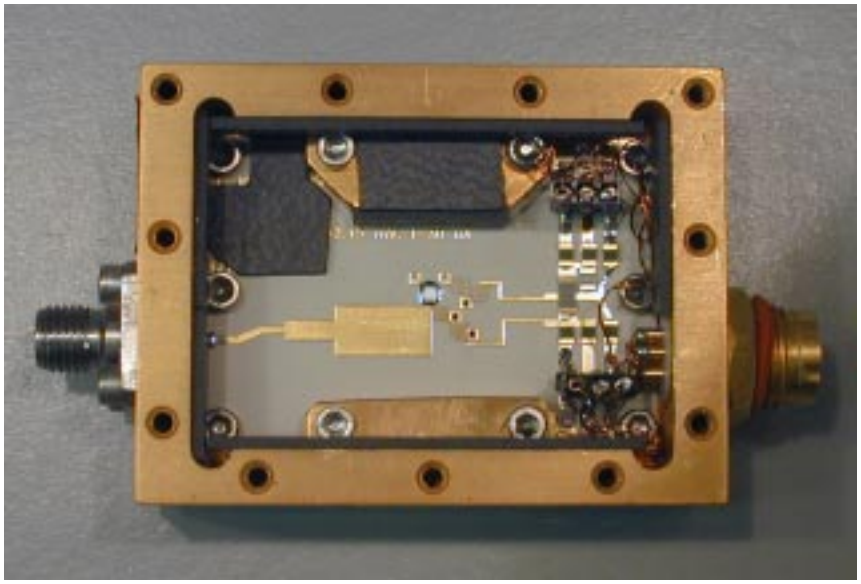

Fig. 10. The mounted SIS mixer chip and IF matching circuit board. The SIS chip is the small black rectangle in the center. The circuitry to the right of the chip is for DC bias. The IF matching circuit is to the lower left of the chip, connected to the SMA connector through a 50 Ω line. The black strips are ferrite absorbers.

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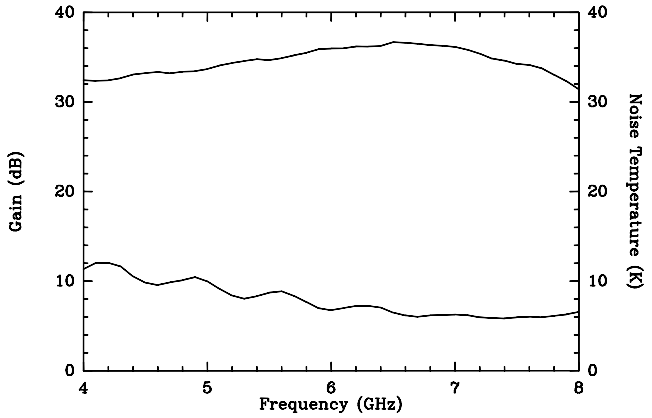

Fig. 11. Gain and noise temperature of the QMMIC LNA, measured at 4.2 Kelvin. The top curve is the gain, and the bottom the noise temperature.

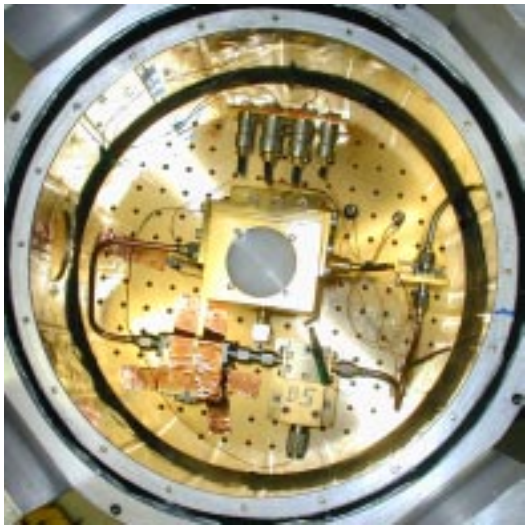

Fig. 12. Cryostat cold surface. The RF and LO signals enter from above, go through the polyethylene lens in the center, and enter the mixer block. The IF signal goes out the coax cable to the left, through the isolator (under copper tape), through the LNA, and out the dewar to the upper right.

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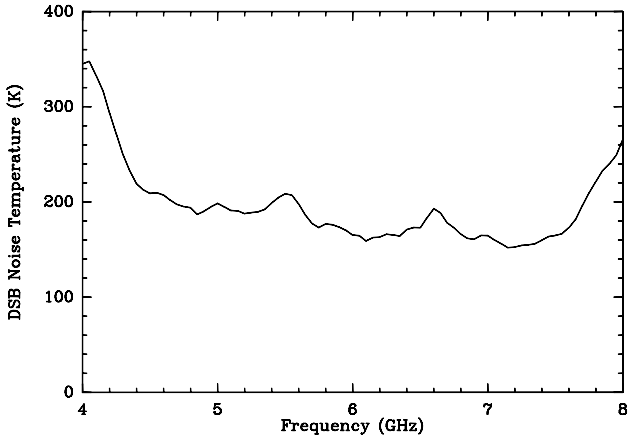

Fig. 13. Noise temperature of the receiver as a function of IF frequency. The LO frequency is 648 GHz, $V_{SIS} = 2.18$ mV, and $I_{SIS} = 59\mu$A.

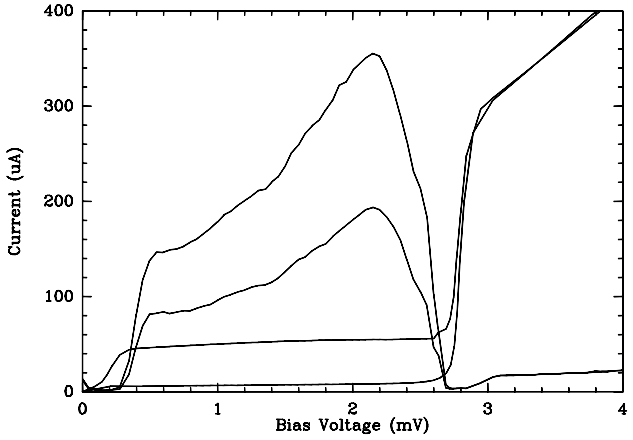

Fig. 14. Unilluminated and pumped IV curves with hot and cold total power. The LO frequency is 630 GHz.

Fig. 15. Receiver mounted at the Cassegrain focus of the CSO. The receiver is in a downward-looking cryostat at the top of the photo. The 690 GHz LO chain is on the front of the cryostat. The rack at the bottom of the photo houses, from left to right, the SIS bias box, magnet bias box (for Jospheson oscillation suppression), LNA bias box, and 4 to 8 GHz IF system.

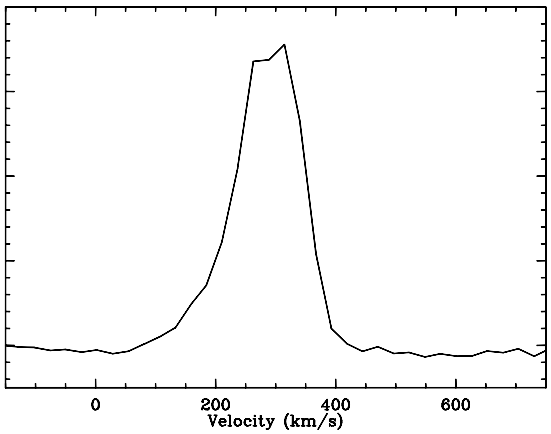

Fig. 16. Spectrum of the J=6 → 5 emission line of carbon monoxide in the galaxy M82. The displayed velocity scale corresponds to a bandwidth of just over 2 GHz.